All-MOS self-referenced temperature sensor

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This Letter presents an all-MOS self-referenced temperature sensor, intended for thermal compensation of dark current in CMOS image sensors (CIS). Its thermal sensing front-end is based on a self-biased nMOS pair working in the subthreshold region. Biased with ratiometric currents, the differential voltage output of the nMOS pair is proportional to the absolute temperature. The thermal sensing voltage is quantised by a self-referenced first-order incremental delta–sigma ADC, which obtains its reference voltage from the thermal sensing front-end. This reference voltage has been virtually attenuated, through switch capacitor charge sampling, to improve the resolution of the temperature sensor. Measured between −20 and 80°C, the proposed temperature sensor achieves an inaccuracy within ±0.55°C.

Introduction: A CMOS image sensor (CIS's) dark current correlates with the electron-hole pair generations, which, in turn, are functions of intrinsic carrier concentration, n_i, which doubles with every 11°C of temperature rise. Therefore, the dark current could be compensated using on-chip temperature sensors [1]. For this purpose, the temperature sensors have to meet the following requirements: (1) incurring no penalty to the image sensing quality; (2) having an accuracy better than 1°C, as dark current increases by ∼15% for every 1°C of temperature rise [2]; (3) Their calibration effort as well as power and area consumptions should be kept to a minimum, as they are auxiliary, instead of main functioning blocks on a CIS chip. To meet (1), a MOS-based temperature sensor is better than a BJT-based alternative, which, when forward biased, incurs electro-luminescence to the nearby image sensors implemented on the same chip [3]. Compared an earlier all-MOS approach [4], this Letter presents a sensor design with the following features: (i) The thermal sensing devices are nMOS, rather than the dynamic threshold pMOS devices whose body and drain are grounded [4]. (ii) Our delta–sigma ADC's reference voltage has been virtually attenuated from V_{GS1} to 1/5 V_{GS1}, through a slight modification of its charge sampling method, to improve its resolution, by a factor of 5, rather than, e.g. using a zoom ADC to improve its resolution [4]. In addition, our temperature sensor can be calibrated at one temperature point, while maintaining its accuracy for the target application.

Operating principle and circuit implementation: The BJT-free thermal sensing front-end is shown in Fig. 1. The op amp forms a negative feedback loop with M_{P1} and M_{P2}, ensuring $V_2 = V_{GS1}$ when its offset can be neglected. The differential output voltage ΔV_{GS} can be expressed as

$$\Delta V_{GS} = \frac{nkT}{q}\ln(N), \tag{1}$$

where $N = 8$ is the current density ratio between M_{N1} and M_{N2} (realised by their area ratio). k is the Boltzman constant; q is electron charge while n is a process dependent factor.

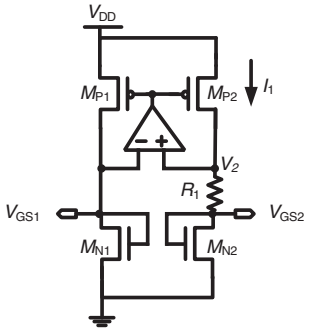

Fig. 1 *Schematic diagram of the thermal sensing front-end*

Non-ideal factors and one-point calibration: The first non-ideal factor is the op amp's offset. Rather than adding a voltage offset to the sensor output, it changes the currents in both sensing devices. By elaborate design, e.g. smaller V_{GS}–V_{TH} of the op amp input pair, which is in the subthreshold region, V_{OS} can be kept low enough for the target accuracy (e.g. 1°C). To investigate the process variations in ΔV_{GS} caused by aforementioned non-idealities, Monte Carlo simulations have been performed for the circuit shown in Fig. 1. The simulation results between − 20 and 80°C, are plotted in Fig. 2. The untrimmed 3 sigma (3σ) process variations are ±0.9% (Fig. 2*a*). This can be reduced to within ±0.8°C, by calibrating at one temperature point, e.g. 30°C (Fig. 2*b*). The one-point calibration procedures are as follows. First of all, the simulated ΔV_{GS} from 100 Monte Carlo simulations are stored (e.g. in MATLAB). Secondly, each temperature sensor's output at 30°C is trimmed to the same value (e.g. 52 mV in Fig. 2) when assigned an individual gain correction factor N_C [1]. After applying the correction factor N_C to each sensor over the temperature range, a second-order master curve fitting is applied to all the sensors.

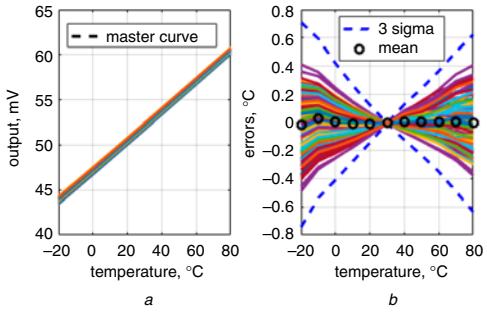

Fig. 2 *100 Monte Carlo simulations of the transistor-level thermal sensing front-end shown in Fig. 1*

a Simulated outputs ΔV_{GS}
b Errors after an individual one-point calibration followed by a second-order master curve fitting

Delta–sigma ADC: Fig. 3 shows the single-ended schematic diagram of the proposed self-referenced first-order delta–sigma ADC, in reference to [5]. In practice, it is a differential circuit. During phase 1, a charge of $5C{\cdot}\Delta V_{GS}$ is sampled on the differential input. During phase 2, the sampled charge is $5C{\cdot}V_{GS1}$ when D_{out} is high, or $4C{\cdot}V_{GS1}$ when D_{out} is low. Thus, the output bitstream at V_{comp_out} represents the ratio of $5C{\cdot}\Delta V_{GS}/V_{GS1}$, which should always be less than unity over the temperature range of interest. This modified delta–sigma modulator (Fig. 3) improves the resolution of the sensor, by a factor of 5 (when the resolution is limited by the ADC, as in this Letter), without adjusting the design parameters (e.g. op amp gain, number of bits) of the delta–sigma ADC or its decimator filter, compared to its alternative of using V_{GS1} as the voltage reference. The mismatches between *4C* and *C* introduces a gain error, which could be trimmed out by the aforementioned one-point calibration. In the TT simulation corner, the op amp *A*1 has a gain of 84 dB and a unity gain bandwidth (UBW) of 23 MHz, given a 1 pF load.

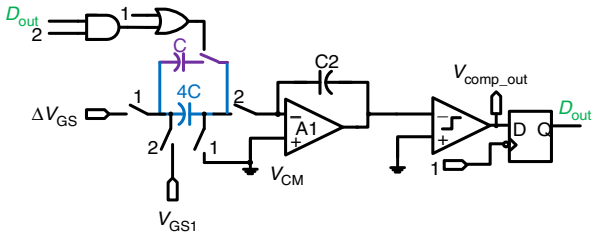

Fig. 3 *Schematic diagram of the proposed delta–sigma ADC for digitising the thermal sensing front-end shown in Fig. 1*

Measurement results of the delta–sigma ADC: The temperature sensor is fabricated using a 0.18 µm CIS technology, together with a CIS chip, as shown in Fig. 4. The active dimensions of the thermal sensing front-end 'nMOS pair & bias' and the ADC are 250 µm × 80 µm and 80 µm × 120 µm, respectively. For flexibility, the decimator filter (a 13 bit counter) is implemented off-chip. The delta–sigma ADC has a 2 $V_{p\text{-}p}$ full scale, and is measured at a 2 MHz, with a 100 $mV_{p\text{-}p}$ (−26 dB) sine wave input at 349 Hz. The measurement results of the differential non-linearity (DNL) and the integral non-linearity (INL) are shown in Fig. 5. Fig. 6 shows the modulator's Fast Fourier transform (FFT) under the same sine wave test after filtered by the 13-bit counter.

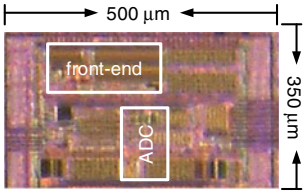

Fig. 4 *Micrograph of the proposed temperature sensor*

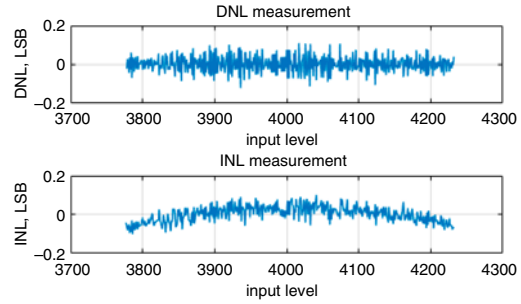

Fig. 5 *Measured DNL and INL of the delta–sigma ADC shown in Fig. 3*

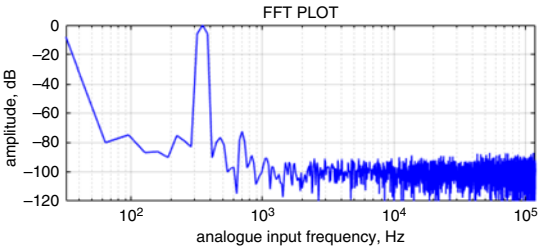

Fig. 6 *Measured FFT plot of the delta–sigma ADC shown in Fig. 3*

Measurement results of the temperature sensor: The proposed temperature sensors have been measured between − 20 and 80°C on 5 different chips, and the results are shown in Fig. 7. Their outputs change by ~600 digital numbers over the 100°C temperature range, as shown in Fig. 7*a*. It dissipates 40 µW, and achieves a resolution of 0.16°C with a conversion time of 4 ms. The noise of the sensor is measured to be 21 µV, or equivalently 0.13°C, which is smaller than the resolution, and hence not limiting its resolution. When the sensors are calibrated at two temperature points at −10 and 70°C, both their gain and offsets mismatches can be sufficiently suppressed, resulting in a 3σ inaccuracy of ±1.05°C (Fig. 7*b*). With a one-point calibration and a second-order master curve fitting, the 3σ inaccuracy becomes ±2.5°C (Fig. 7*c*).

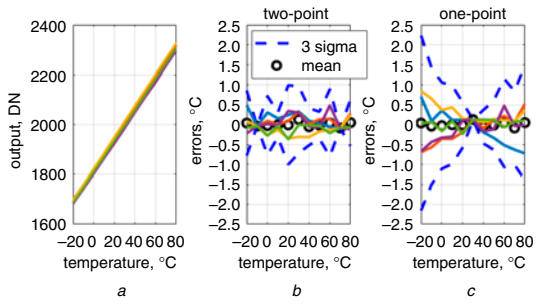

Fig. 7 *Measurement results of the temperature sensor*

a Digital outputs of the temperature sensors from 5 chips
b Measurement errors, after a two-point calibration at − 10 and 70°C
c and after a one-point calibration at 30°C for each sensor. Both b and c are upon a second-order master curve fitting for all the sensors

Conclusions: An all-MOS self-referenced temperature sensor, which is intended for CIS's dark current compensation, has been fabricated using a 0.18 µm CIS technology. Based on the measurement results from 5 chips, its 3σ inaccuracy is within ±1.05°C between −20 and 80°C after a 2-point calibration. It is compared with the state-of-the-art works listed in Table 1.

Table 1: Performances compared with the state-of-the-art works

	This work	[6]	[7]	[8]
sensor type	MOS	MOS	MOS	MOS
CMOS technology	0.18 µm	65 nm	28 nm	0.18 µm
area, µm^2	29,600	4000	1000	89,000
temperature range	−20 to 80°C	0 to 100°C	−5 to 85°C	−20 to 80°C
3σ accuracy	±1.05°C	±2.3°C	−3.3/1.9°C	±1°C
calibration	Two-point	Two-point	One-point	Two-point
power consumption, µW	40	154	56	0.8
conversion time, ms	4	0.022	0.036	800
resolution, °C	0.16	0.3	0.76	0.09
resolution FOM, nJ·K^{2}[a]	4	304.9	1.2	5.3
rel.IA, %[b]	2.1	4.6	5.8	2

[a]Energy/Conversion × (Resolution)^2, in reference to [9].
[b]3σ accuracy/temperature range, in reference to [9].

The advantages of our design are a reasonably low FOM, when fabricated using a conservative (cost effective) technology.

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One or more of the Figures in this Letter are available in colour online.

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